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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDREI TERECHKO

Appeal 2009-004042
Application 10/552,076
Technology Center 2100

Decided: September 25, 2009

Before LEE E. BARRETT, LANCE LEONARD BARRY, and HOWARD B. BLANKENSHIP, *Administrative Patent Judges.*

BLANKENSHIP, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-8, which are all the claims in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse the Examiner's rejection, *pro forma*, and enter a new ground of rejection as permitted by 37 C.F.R. § 41.50(b).

Invention

Appellant's invention relates to Instruction Level Parallelism (ILP) processors, and in particular Very Large Instruction Word (VLIW) architecture.

Representative Claim

1. Data processing system comprising:

- a clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;

- an instruction unit for issuing control signals to said clusters, wherein said instruction unit is connected to each of said clusters via respective control connections, and

one or more additional pipeline registers is arranged in said control connections depending on the distance between said instruction unit and said clusters, said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters.

Prior Art

Nickolls	5,598,408	Jan. 28, 1997
Pechanek	5,659,785	Aug. 19, 1997
Batten	6,269,437 B1	Jul. 31, 2001

Examiner's Rejections

Claims 1-3 and 5-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Batten and Nickolls.

Claims 4 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Batten, Nickolls, and Pechanek.[1]

DISCUSSION

I.

The Standing Rejections

We reverse, *pro forma*, the Examiner's rejection of the claims over the prior art, because the claims are indefinite under 35 U.S.C. § 112, second paragraph. Rejections of claims over prior art should not be based on speculation and assumptions as to the scope of the claims. *See In re Steele,* 305 F.2d 859, 862 (CCPA 1962). We enter a new ground of rejection against all the claims on appeal, *infra*.

II.

Definiteness

The function of claims is (1) to point out what the invention is in such a way as to distinguish it from the prior art; and (2) to define the scope of protection afforded by the patent. *In re Vamco Machine & Tool, Inc.*, 752 F.2d 1564, 1577 n.5 (Fed. Cir. 1985). The legal standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope. *In*

[1] The Examiner is correct in that the objection to the title of the invention, argued by Appellant in the Appeal Brief as a ground of rejection for our review, is a matter for petition. *See Manual of Patent Examining Procedure* §§ 706.01, 1002.02(c), and 1201 (Eighth ed., Rev. 7, Jul. 2008).

re Warmerdam, 33 F.3d 1354, 1361 (Fed. Cir. 1994). The inquiry is merely to determine whether the claims do, in fact, set out and circumscribe a particular area with a reasonable degree of precision and particularity. *In re Moore*, 439 F.2d 1232, 1235 (CCPA 1971). The definiteness of the language employed must be analyzed -- not in a vacuum, but in light of the teachings of the prior art and of the particular application disclosure as it would be interpreted by one possessing the ordinary level of skill in the pertinent art. *Id.*

New Ground of Rejection -- 35 U.S.C. § 112, Second Paragraph

We reject claims 1-8 under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1 and 5 are independent. We will discuss claim 1 as representative of the independent claims.

The final portion of claim 1 recites, "one or more additional pipeline registers is arranged in said control connections depending on the distance between said instruction unit and said clusters, *said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters*" (emphasis added).

According to Appellant, the subject matter of claim 1 (and claim 5) is described at Figure 1 and page 4, lines 18 through 29 of the Specification. Br. 3-4.

Appellant's disclosure describes a pipeline register P (Figure 1) arranged in control connections, depending on the distance between the instruction unit (IFD) and clusters C and D. The disclosure also describes five pipeline registers P, as depicted in Figure 1, one of which appears in each connection between clusters A, B, C, and D.

The Examiner entered a final rejection against the claims under 35 U.S.C. § 112, second paragraph, which was withdrawn in the Answer. However, we have substantially the same concerns as did the Examiner. The claim is ambiguous with respect to how, or if, the pipeline registers being "adapted to provide a dedicated direct signal data signal connection between any two of said clusters" are the same as the "one or more additional pipeline registers" arranged in the control connections.

In response to the § 112 rejection, Appellant did not attempt to explain how the "pipeline register" limitations are to be interpreted. Appellant, instead, reproduced text from the Specification and alleged that "[f]rom the description in the filed application in which the signal connection featured in claim 1 is provided verbatim, one can garner how the dedicated signal connection is realized." Br. 7. Appellant did not explain or elaborate on how one might "garner."

We reproduce the relevant section of the Specification below, although our emphasis differs from that provided by Appellant in the Appeal Brief.

> In Fig. 1 a clustered VLIW architecture *with a full point-to-point connectivity topology* according to a first embodiment is shown. *The architecture includes four clusters*, namely clusters A, B, C and D, *which are fully connected to each other* and an instruction fetch/dispatch unit IFD being connected to each cluster A-D via control connections paths CA-CD. *Accordingly, there is always a dedicated direct data signal connection present between any two clusters with pipeline registers P arranged between each two clusters.* The latency of an inter-cluster transfer of data is always the same for every inter-cluster connection independent of the actual distance between the clusters on the chip. The actual distance on the chip between the clusters A and C, and clusters B and D is

> considered to be longer than the distance between the clusters A and D, A and B, B and C, as well as C and D. *Therefore, a pipeline register P is arranged in the control connection paths CC and CD, in order to pipeline the control signals to remote clusters C, D.*

Spec. 4:18-29 (emphasis added).

In a careful reading of the material at page 4, and in view of the earlier description of a "dedicated direct connection" between clusters due to "full point-to-point connectivity topology" in the first full paragraph of Specification page 2, Appellant appears to describe a "dedicated direct data signal connection" by means of the direct connections between the clusters shown in Figure 1, which have a pipeline register in each connection.[2] Note that the "dedicated direct data signal connection present between any two clusters" is established at page 4 before any mention of the pipeline register in the control connection paths CC and CD (i.e., "[a]ccordingly, there is always" comes before the discussion of the pipeline register in the control paths).

The pipeline register in the *control connection* paths, *in order to pipeline the control signals*, is not described as being adapted to provide a *dedicated direct signal data signal* between any two of the clusters. At best, the five pipeline registers in the direct connections between the clusters may be "adapted to provide" a dedicated direct data signal connection between any two of the clusters. However, the five pipeline registers are not arranged in the control connections, and are greater in number than the one, two,

[2] Although of lesser importance, it is unclear what the claimed "dedicated direct signal data signal connection" might be, when the disclosure describes a "dedicated direct data signal connection." Appellant claims more "signals" than described.

three, and four pipeline registers covered by a recitation of "one or more" pipeline registers.

We conclude that one skilled in the art cannot reasonably ascertain how, or if, the same pipeline register or registers are both arranged in the control connections and somehow "adapted to provide" a dedicated direct signal data signal connection between any two of the clusters. The claims thus fail to pass muster under 35 U.S.C. § 112, second paragraph.

DECISION

The Examiner's rejection of claims 1-8 under 35 U.S.C. § 103(a) is reversed, *pro forma*.

In a new ground of rejection, we reject claims 1-8 under 35 U.S.C. § 112, second paragraph, as being indefinite.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) (2009). 37 C.F.R. § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

REVERSED -- 37 C.F.R. § 41.50(b)

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